NEW DEVELOPMENTS WITH INTEGRATED FIN-LINE AND RELATED PRINTED MILLIMETER CIRCUITS

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Abstract

New examples of integrated fin-line and related printed millimeter circuits are presented as a further demonstration of the advantages of such construction techniques. The circuits include a wideband matched PIN attenuator, single-ridged and monopole-coupled semiconductor mounts, and an integrated receiver front end.

Introduction

Integrated fin-line (references 1 through 3) is believed to be a transmission line with great potential in millimeter applications by virtue of its compatibility with active and passive hybrid devices, freedom from stringent tolerances, low-cost reproducibility, and reasonable insertion loss. The following paragraphs show recent progress in development of components constructed with integrated fin-line and related printed-circuit techniques.

Fin-Line Attenuators

Although the performance of the first PIN attenuator constructed in fin-line (reference 3) was gratifying, the preliminary demonstration was limited in terms of bandwidth and forward-bias rejection. To better illustrate the full potential of fin-line PIN attenuators, the model shown in Figure 1 was constructed and tested. The housing is similar to that described previously, except for the inner dimensions (0.112 × 0.224 in. for WR-22 instrumentation) and the alignment of internal components (Rexolite dowels rather than nylon screws). This construction technique, in conjunction with more homogeneous printed-circuit boards such as irradiated polyolefin (reference 4), is expected to be useful in fin-line circuits beyond 100 GHz. Current work, however, has been limited to addressing immediate applications from 26.5 through 50.0 GHz where a fiber-filled dielectric (0.010 in. Duroid 5880) has proved to be adequate. The housing, which is amenable to simple machining or casting operations, provides two parallel-plate regions. One of the parallel-plate regions accommodates a printed RF blocking network for the bias circuit, which exits through a 3-mm coax connector. The printed circuit board, insulating gasket, and grounding shim can all be manufactured in volume by punching operations, thereby providing a significant cost advantage over those competing IC techniques which require the grinding and polishing of refractory materials.

The performance of the new fin-line PIN attenuator is summarized in Figure 2. Across the band from 33 through 44 GHz, the forward-bias rejection is 30 ± 5 dB and the reverse-bias loss is 1.4 ±0.2 dB. The sketch in the upper part of Figure 2 shows how the four PIN diodes (Alpha DSG-6474A) were grouped to provide a tapered loading to the fin-line and thereby minimize the VSWR over a wide range of bias conditions. Across the 29-percent design band, the measured VSWR of the four-diode attenuator is less than 1.5 for attenuation levels up to 10 dB and less than 2.0 for attenuation levels up to 17 dB.

Several two-diode versions of fin-line attenuators (each containing two diodes spaced a quarter-wave apart) were also developed for parametric amplifier pump-leveling applications. One version of the two-diode attenuator, optimized for the upper portion of the WR-22 band, provided a reverse-bias loss of 0.95 ±0.25 dB and forward-bias rejection of 14.1 ±0.7 dB across the band of 40 to 50 GHz. The excellent performance observed at 50 GHz supports the equivalent-circuit analysis (reference 3) which has predicted that commercially available PIN diodes can be utilized in simple fin-line mounts at frequencies well above 100 GHz.

Semiconductor Mounts

Figure 3 shows two new printed-circuit semiconductor mounts which are compatible with fin-line structures and introduce less video-bypass capacitance than the double-ridged mount utilized in the PIN attenuator. The low capacitance mounts are preferred for mixer applications, particularly those requiring high IF's. The monopole-coupled circuit appearing in the upper part of Figure 3 was optimized in a WR-28 housing similar to that shown in Figure 1. The signal and the local oscillator (LO) enter the circuit from the left and are coupled to a beam-lead GaAs Schottky barrier diode (AEI DC-1306) by a low-impedance monopole. The latter is terminated, a quarter-wave away, by a short-circuit bifurcation of the waveguide housing. The upper portion of the bifurcation, which is insulated from the housing by the same gasket that insulates the IF output, is slotted to prevent a TEM resonance within the waveguide-wall choke region. (Although such slots are required in low-loss asymmetrical structures, they do not appear to be necessary in the double-ridged configuration, particularly where PIN diodes provide resistive damping.) The IF output from the monopole is extracted through an RF blocking network consisting of a quarter-wave low-impedance line within the waveguide wall, followed by cascaded quarter-wave sections of high and low impedance lines. Since the latter lines are located in the parallel-plate section of the housing, they are actually part of a suspended-substrate stripline. The dimensions of the monopole were experimentally varied to optimize the impedance match between the WR-28 input and the mixer diode under typical LO drive conditions (1 mW of

LO power combined with 1.5 mA of dc bias). A VSWR of 2.0 or better was achieved across a 4-GHz band centered near 35 GHz. Noise-figure measurements were performed by connecting a noise generator (AIL Type 07096) and a klystron LO to the main and decoupled ports, respectively, of an external directional coupler. The IF port was connected to a 50-ohm 1.3-GHz preamplifier, a second mixer, and a 30-MHz precision test receiver. Measurements showed a double-sideband noise figure of 8 to 10 dB (depending upon the diode sample, LO frequency, and drive level) including a 3-dB IF contribution. The results are gratifying as the mixer diode had been specifically designed for operation in the band of 12 to 18 GHz, and no attempt was made to optimize the IF impedance match.

A second low-capacitance semiconductor mount is shown in the lower part of Figure 3. This single-ridged fin-line mount was optimized in another WR-28 fixture, with the signal and LO entering from the right. The DC-1306 diode is mounted across a low-impedance section of single-ridged line which is terminated, a quarter-wave away, in a printed short circuit. The diode is matched by a multiple-wave-length taper combined with a lumped negative-capacitance element (formed by a notch within the ridge). Impedance measurements under typical LO-drive conditions show a VSWR of 2.0 or better across a 5-GHz band centered near 34 GHz. It is believed that a considerably wider bandwidth could be obtained with multiple quarter-wave transformers substituted for the notch-taper configuration.

Integrated Receiver Front End

Figure 4 shows a millimeter receiver front end which was printed on a single board and tested in a WR-28 housing similar to that presented in Figure 1. The front end contains a monopole-coupled mixer and two band-pass filters which diplex the signal and LO ports. A similar receiver configuration has been constructed on a copper sheet without dielectric backing (reference 5) for operation at X-band. The circuit of Figure 4 offers the ability to print the diode mount, and its associated RF-blocking and bias networks, at the expense of unloaded resonator Q. Inductive filter elements are printed on both sides of the board to achieve the high susceptance ($jB/Y_0 \geq 10$) required for typical diplexing applications. The inductive strips are generally terminated in longitudinal rails which rest against metal surfaces in the Figure 1 assembly; no rail exists in the insulated region to preclude a TEM resonance. The signal and LO band-pass filters are equal-element designs (reference 6), each containing two sections.

Figure 5 is a plot of the insertion loss of each band-pass filter, measured prior to the receiver integration. Each filter has a 3-dB bandwidth of 1.8 GHz and a midband insertion loss of 0.7 dB. Although the passband centers are spaced 2.0 GHz apart, the two-element response can accommodate any IF between 1 and 3 GHz. Assuming the signal and LO frequencies are 33.25 and 35.25 GHz, respectively, the LO band-pass filter will provide a highly reactive termination (16-dB rejection) to the mixer at the RF frequency. The LO-to-RF rejection should be about 18 dB, with 12.5 dB provided by the signal filter and approximately 6 dB lost in the impedance-matched mixer. The image at 37.25 GHz will be reactively terminated (11.5 to 19.0 dB rejection) by both filters. Greater rejection can be obtained at the expense of midband loss, which is generally of minor concern in the LO channel. Further improvements in selectivity can be obtained by increasing the number of sections in each filter and/or reducing the cutoff frequency of the waveguide housing.

After demonstrating satisfactory performance for the signal and LO band-pass filters, these components were integrated with the previously described monopole mixer to form the complete receiver front end of Figure 4. The spacing between the monopole and the LO filter was varied to optimize the impedance match between the signal port and the mixer and, in the interest of schedule limitations, an equal spacing was arbitrarily utilized between the signal filter and the monopole. Noise-figure measurements, performed with a 50-ohm, 1.3-GHz, IF amplifier, showed that the receiver had a single-sideband noise figure of 12.6 dB, including a 3-dB IF contribution. It is believed that the noise figure could be significantly reduced by incorporating a mixer diode with a higher cutoff frequency, optimizing the phase of the image termination, and impedance matching the mixer/IF interface.

Summary

The previous examples of low-cost printed millimeter circuits have been presented as a further demonstration of the versatility of integrated fin-line and related construction techniques. These techniques offer compatibility with chip and beam-lead devices, freedom from stringent tolerances, low-cost reproducibility, and reasonable insertion loss at millimeter wavelengths.

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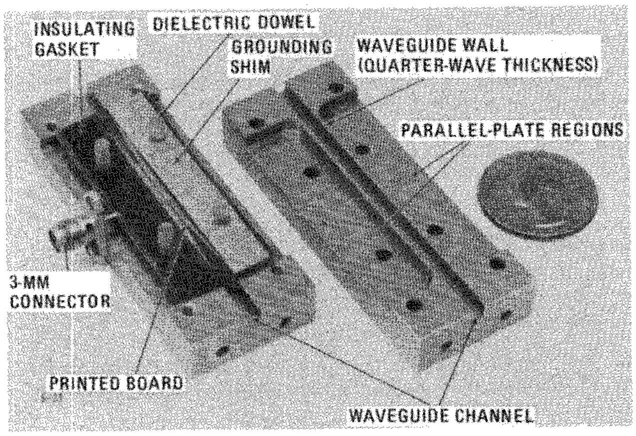

FIGURE 1. IMPROVED FIN-LINE HOUSING

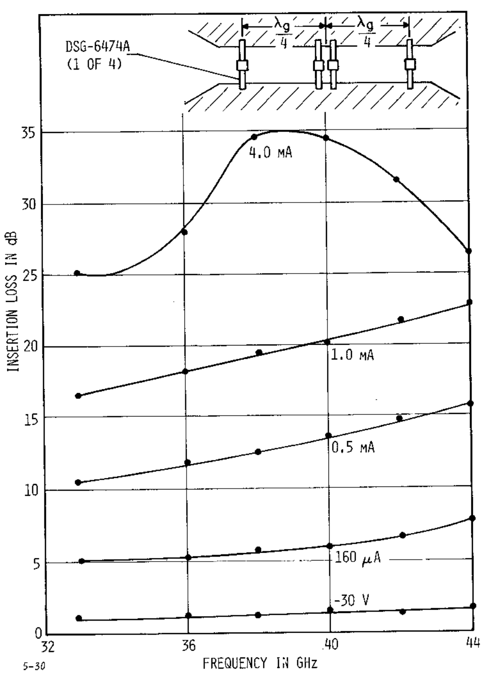

FIGURE 2. PERFORMANCE OF PIN ATTENUATOR

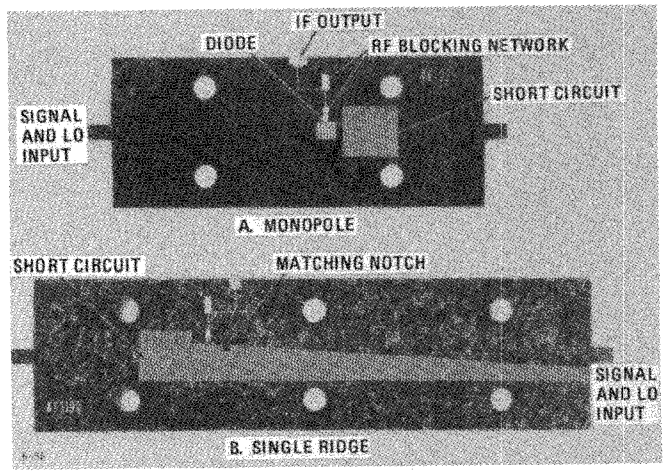

FIGURE 3. PRINTED-CIRCUIT SEMICONDUCTOR MOUNTS

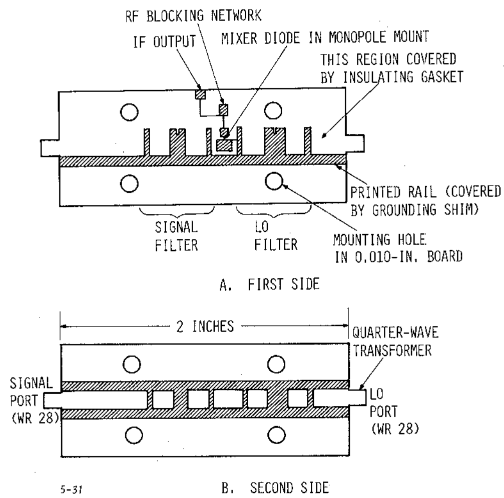

FIGURE 4. INTEGRATED RECEIVER FRONT END

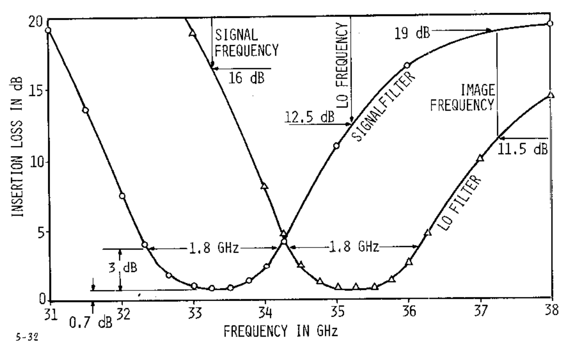

FIGURE 5. FILTER RESPONSE CURVES